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1. Introduction

This single width CAMAC module acts as a Master (or Slave) Node for an Intel BITBUS (TM) Network. Full facilities are included for transmitting and receiving messages, and memory sites are available for program and data stores. The considerable assistance of staff at NIKHEF, Holland in the design and implementation of this module is gratefully acknowledged.

2. Features and Facilities

8044 BITBUS Enhanced Microcontroller processor, 12MHz clock.

Asynchronous (Self-clocked) opto-isolated RS 485 serial port at 62.5 or 375 Kbits/sec. with Repeater support.

32K x 8 (62256) SRAM/EPROM site for firmware or down-loaded code.

32K x 8 (62256) SRAM site for data storage

(Both memory sites may be fitted with smaller devices if desired)

** Diagnostic Mode for putting the 8044 "OFF Line" and writing/reading the on-board memory areas/switches/FIFOs etc.
using a 16-bit writeable/readable pointer.

** 9-bit Transmit FIFO 512 bytes deep

** 9-bit Receive FIFO 512 bytes deep

(Other FIFO depths available)

** Full Message/FIFO Control Logic

** 8-bit BitBus Node Address select switch

** 8-bit Configuration select switch

** Full Dataway Command decode

3. Operational Description

The main function of this unit is to permit a CAMAC Host/controller to send and receive messages to and from the 8044 BITBUS processor in this module so that remote BITBUS nodes can be instructed to perform tasks, output or collect data and send replies.

The module operates in two principal modes: Normal and Diagnostic.

3.1 Normal Mode:

In Normal Mode, the unit uses the FIFOs to pass data between the processor and the CAMAC port, with flags signalling "Data Ready" at the Receive (RX) port and "Space Available" at the Transmit (TX) port.

In Normal Mode the module responds to the following commands:-

Command	Description	X	Q
F(0) A(1)	Read RX FIFO	1	Data Ready
F(1) A(12)	Read Status Register	1	0

The Status Register shows Processor and FIFO status:

Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
TFNF	/TFNE	/RFNF	RCMD	RFNE	/DIAG.	P1.1	P1.0

TFNF Transmit FIFO not Full ('1' = not full)
 /TFNE Transmit FIFO Empty ('1' = TX FIFO empty)
 /RFNF Receive FIFO Full ('1' = RX FIFO full)
 RCMD Command Byte of Receive Message detected ('1'=TRUE)
 RFNE Receive FIFO not empty ('1' = RX FIFO not empty)
 /DIAG. Diagnostic Mode ('1' = Normal, '0' = Diagnostic)
 P1.0, 1.1 Processor Status

F(8) A(15)	Test LAM output	1	Q = LAM set
F(16) A(0)	Write TX FIFO	1	T.FIFO not full
F(24) A(0)	Disable TX Empty LAM	1	0
F(24) A(1)	Disable RX Command LAM	1	0
F(24) A(15)	Disable processor, enter Diagnostic Mode	1	0
F(25) A(15)	RESET - Reset processor, clear flags, enter Normal Mode.	1	0
(RESET is given internally at Power On)			
F(26) A(0)	Enable TX Empty LAM	1	0
F(26) A(1)	Enable RX Command LAM	1	0
F(27) A(0)	Test TX Empty LAM Enabled	1	Q=Enabled
F(27) A(1)	Test RX Command LAM Enabled	1	Q=Enabled

3.1.1 FIFOs Flags and LAMs (see also Section 4.)

Each of the FIFOs has an Empty and a Full flag. All four are visible through the Status Register. RFNF and TFNE are presented to the 8044 processor to tell it respectively that it may output bytes to the receive FIFO and that bytes are available to read from the transmit FIFO, signalled by it not being empty. On the CAMAC side, either of two flags, each of which has its own enable/disable flag, may give rise to a LAM (module 'Look-At-Me' = Interrupt) output. The flag associated with the TX path says simply that the TX FIFO is empty, so a complete message may be written from CAMAC into the TX FIFO to be transmitted by the 8044 processor to a remote Node. On the RX side, logic detects when the processor writes a Command Byte (see below) into the RX FIFO, signalling the end of a message which is now ready to be read out. This flag is reset by the CAMAC port reading the RX FIFO at the time when the Command byte is output.

3.1.2 Data Format

The data path between CAMAC and the 8044 is two FIFOs 9 bits wide with 8 data bits and the ninth bit being used to flag a command byte. Command bytes are added to the end of all BITBUS messages and, in the case of the Transmit path, logic detects when the ninth bit has been written as '1' to tell the processor via a signal called TCMD (Transmit Command) that a command byte is in the TX FIFO. The TCMD flag is reset when the 8044 processor reads the TX FIFO at the Command FIFO address FF01 instead of the Data FIFO address FF00. The Q response of the module to the Write TX FIFO command is '1' until the FIFO is full.

When the 8044 processor writes a command byte to the receive FIFO, by writing to FF01 instead of FF00, logic detects this and sets the RCMD (Receive Command) flag which is visible in the Status Register and may also set LAM. This means that a complete message has been written into the RX FIFO. As the data is read out (F(0) A(1)), bit 9 identifies data/command ('1' = Command) and Q='1' is given until all bytes have been read out.

3.2 Diagnostic Mode

This mode is intended as a test feature, and entering the mode with the command F(24) A(15) disables the processor and allows complete access to the memory and I/O areas from CAMAC. The memory address used is stored in a 16-bit auto-incrementing pointer register which may be written and read:-

	X	Q
F(1) A(0) Read Diagnostic Pointer	1	0
F(17) A(0) Write Diagnostic Pointer	1	0

The standard data read and write commands F(0) and F(16) now allow the CAMAC controller to write and read the 8044's memory and I/O at the address stored in the pointer, with the pointer incrementing after each command. For testing a single location, this incrementing can be turned off:

	X	Q
F(24) A(2) Disable Pointer Increment	1	0
F(27) A(2) Test Pointer Increment Enabled	1	Enabled

(The pointer increment is automatically enabled on entry to diagnostic mode, so no command is needed to enable the feature).

4. Memory Map

Address	Contents	Notes
FFFF	Node Address Switches	8 bits
FFFE	Configuration Switches	8 bits
FF01	Command Byte FIFO) = Data FIFO + Flag
FF00	Data Byte FIFO) see Note 1 below
8000-FFFF	Program Memory)
0000-7FFF	Data Memory) see Note 2 below

Note 1: The 8044 processor expects there to be a total of four FIFOs in a master node configuration as used in this module; that is Transmit Command, Transmit Data, Receive Command and Receive Data. This module uses just two FIFOs, with the Data/Command FIFO selection through the least significant address bit (FF00/FF01) and data/command bytes identified by the ninth bit as described above.

(In Normal Mode, TX and RX FIFOs are at the same address(es), the 8044 processor reads from the TX FIFO and writes to the RX FIFO. In diagnostic mode they are separated, so that both may be written and read from CAMAC; the TX FIFO remains at FF00/1, the RX FIFO moves to FF80/1).

Note 2: The 8044 processor maintains two memory maps, one for Code (i.e. Program Space) and one for Data (i.e. Random Access Memory and I/O). This module is fitted as standard with 32K of RAM in each area as shown above. Notice how the top of the Program Memory appears to conflict with the FIFOs and Configuration/Node Address switches, but they do not, of course, since they are in different "Processor Spaces".

5. Communications

The unit communicates with the BITBUS network over an RS 485 connection, which will operate as standard at 62.5 or 375 Kbits/second asynchronous. In addition, opto-isolation is included to separate the unit from the signal network.

Hytec Electronics also offers a wide range of small remote node assemblies featuring digital inputs/outputs, analogue inputs/outputs and counter channels.

5.1 Message Formats

A full description of BITBUS messages is clearly beyond the scope of this manual, but to give the user an idea of how this module is used, here is a typical message sequence, talking to a remote node at address 80 HEX. The 1360 module is set to address FF HEX.

First we send a "SYS" message to ask the remote node if it is OK and what tasks it is running:-

	Byte TX	Byte RX	Comments
	0F	0F	Tot. message length incl two link bytes
Type	40	C0	Reply bit is set
	80	80	Remote Node Address
Task	00	00	To Task 0 on remote node
Cmd/Rsp.	03	00	Reply Byte = 0 = OK
	00	01	RAC Task is active
Data 2	00	00	
Data 3	00	00	
etc.	00	00	
	00	00	
	00	00	
	00	00	
	00	00	
	100	100	Command byte = 'end of message'

Now we send a message to write some data into external data space on the remote node:-

	Byte	Byte	Comments
	TX	RX	
	14	14	Tot. message length incl. 2 link bytes
Type	40	C0	Reply bit is set
	80	80	Remote Node Address
Task	00	00	To Task 0
Cmd/Rsp.	09	00	09= write external data memory
			Reply Byte = 0 = OK
Data 1	04	04	High byte, ext. memory start address
Data 2	00	00	Low byte, ext. memory start address
Data 3	01	01	
etc.	23	23	
	45	45	
	67	67	
	89	89	
	AB	AB	
	CD	CD	
	EF	EF	
	AA	AA	
	55	55	
	F0	F0	
	100	100	Command byte = 'end of message'

Now we'll send a message to read the data back from external data space on the remote node:-

	Byte	Byte	Comments
	TX	RX	
	14	14	Tot. message length incl. 2 link bytes
Type	40	C0	Reply bit is set
	80	80	Remote Node Address
Task	00	00	To Task 0
Cmd/Rsp.	08	00	08=read external data memory
			Reply Byte = 0 = OK
Data 1	04	04	High byte, ext. memory start address
Data 2	00	00	Low byte, ext. memory start address
Data 3	00	01	
etc.	00	23	
	00	45	
	00	67	
	00	89	
	00	AB	
	00	CD	
	00	EF	
	00	AA	
	00	55	
	00	F0	
	100	100	Command byte = 'end of message'

6. Setting Up

6.1 Code Memory Site Configuration - P1-P5.

As Standard, these links are set up for a 32K x 8 RAM chip, HM62256 or similar.

Link P1 to P5 and P2 to P4.

To fit an EPROM, for example a 27256, proceed as follows:-

Link P1 to P4, link P3 to P5.

Memories fitted in the Data and Code memory sites should have an access time of 150nS or better. Both devices supplied a standard are suitable.

6.2 Repeater Control Enable - JP1, JP2.

As Standard, these jumpers are set for No external Repeaters, meaning that Data Direction is controlled by I/O (In/Out) on the 8044, pin 10. Optionally, the jumpers may be set so that /RTS (Request to Send) controls Data Direction and the /RTS signal is output on the BITBUS connector in order to control remote repeaters.

Fit JP1, omit JP2 : No repeaters.

Fit JP2, omit JP1 : Repeaters used.

6.3 Configuration and Node Address switches.

SW1 sets the BITBUS Configuration; switch element 1 controls the least significant bit (D0), switch element 8 controls the most significant bit (D7). OFF = '1', ON = '0'.

Standard settings:-	Element	Setting	Action
	1	OFF)
	2	OFF) 62.5Kb Asynch. *
	3	ON	reserved
	4	OFF	/EA pin
	5	OFF	Memory decode 'B'
	6	OFF	Byte FIFO fitted
	7	ON	Interrupt Mode FIFOs
	8	ON	reserved

Note * : For 375Kb/Sec. Asynchronous operation, set element 1 to OFF and element 2 to ON.

SW2 sets the Node Address; switch element 1 controls the least significant bit D0 which corresponds to address binary/decimal 1, switch element 8 controls the most significant bit D7 corresponding to decimal 128. OFF = '1', ON = '0'. Standard setting is all OFF which is address FF HEX or 255 decimal.

7. Physical and Electrical

The unit is a single width CAMAC module, with front panel 9-way Cannon socket connector to the network, pinout as follows:-

Pin	Function
1	No connection
2	Signal common (isolated ground)
3	Data -
4	RTS -
5	RGND - 100 ohms to Isolated Ground
6	No connection
7	Signal common (isolated ground)
8	Data +
9	RTS + (Request to Send)

Data +/- is a bidirectional differential self clocked pair, terminated internally in 120 ohms. RTS +/- is similar for Request-to-Send for repeater control.

On the front panel there are LEDs for the following:

2 LEDs (1 red, 1 green) for processor status (standard 8044)

1 red LED for 'N' - Module Addressed (stretched to 20 mSec.)

1 red LED for 'Diagnostic Mode'

1 red LED for RX FIFO Data Present (RFNE)

1 red LED for TX FIFO Data Present (TFNE)

The unit consumes 1.5 amps from the CAMAC Dataway +6V power supply; no other supplies are used.

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8. Parts List Issue C - Issue 2 PCB

PART	TYPE	OUTLINE	COMMENTS
IC1	7401,7401		DIL14
IC2	7401,7401		DIL14
IC3	74244,LS240		DIL20
IC4	74244,LS240		DIL20
IC5	MACH130,MACH130		84PQPS Socket AMD V24
IC6	MK4501,MK4501N-20		DIL28 Socket SGS-T
IC7	7401,7401		DIL14
IC8	7401,7401		DIL14
IC9	74244,LS244		DIL20
IC10	7430,74LS30		DIL14
IC11	7401,7401		DIL14
IC12	MK4501,MK4501N-20		DIL28 Socket SGS-T
IC13	HM62256LP-12)	DIL28 Socket Hitachi
IC14	HM62256LP-12/27256-12)	DIL28 Socket Hitachi
	or equivalents for IC13,14.		
IC15	74593,LS593		DIL20
IC16	74245,LS245		DIL20
IC17	74374,LS374		DIL20
IC18	74244,LS244		DIL20
IC19	PAL18P8,P18P8		DIL20 Socket, any power
IC20	74245,LS245		DIL20
IC21	74373,LS373		DIL20
IC22	7475,74LS75		DIL16
IC23	74593,LS593		DIL20
IC24	74244,LS244		DIL20
IC25	8044,P8044AH-0117		DIL40 Socket Intel
IC26	7404,74LS04		DIL14
IC27	74257,74LS257		DIL16
IC28	74257,74LS257		DIL16
IC29	74123,LS123		DIL16
IC30	7414,74LS14		DIL14
IC31	NME0505S		SIL4 Newport/Farn.DC-DC
IC32	DS75176BN/SN75176BP		DIL8 National/Texas
IC34	HCPL2630,HCPL2630		DIL8 HP
IC33	DS75176BN/SN75176BP		DIL8 National/Texas
IC35	HCPL2630,HCPL2630		DIL8 HP
D1	1N4005,1N4005		DDCMC
D2	1N4148,1N4148		DO35
D3	LED-RED,LED(Red)		LEDBD
D4	LED-GRN,LED(Green)		LEDBD
D5	LED-RED,LED(Red)		LEDBD
D6	LED-RED,LED(Red)		LEDBD
D7	LED-RED,LED(Red)		LEDBD
D8	LED-RED,LED(Red)		LEDBD
XT1	HC18S,12MHZ		XTAL
R1	RESA8,100K		RESA8
R2	RESA8,1K5		RESA8

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PART	TYPE	OUTLINE	COMMENTS
R3	RESA8,47K		RESA8
R4	RESA8,820R		RESA8
R5	RESA8,2K2		RESA8
R6	RESA8,2K2		RESA8
R7	RESA8,100R		RESA8
R8	RESA8,120R		RESA8
R9	RESA8,120R		RESA8
R10	RESA8,1K0	RESA8	
R11	RESA8,100R	RESA8	
C1	CAPR4D4E,47uF/16V		CAPR4D4E
C2	CAPR4D4E,47uF/16V		CAPR4D4E
C3	CAPR4D4E,47uF/16V		CAPR4D4E
C4	CAPR2W2,100PF		CAPR2W2
C5-23	CAPR2W2,100N		CAPR2W2
C24	CAPR4D4E,47uF/16V		CAPR4D4E
C25	CAPR2W2,22pF		CAPR2W2
C26	CAPR2W2,22pF		CAPR2W2
C27	CAPR2W2,100pF		CAPR2W2
C28-C31	CAPR2W2,100N		CAPR2W2
C32	CAPR4D4E,10uF/16V		CAPR4D4E
C33	CAPR4D4E,10uF/16V		CAPR4D4E
C34	CAPR4D4E,47uF/16V		CAPR4D4E
C35	CAPR4D4E,10uF/16V		CAPR4D4E
C36	CAPR4D4E,10uF/16V		CAPR4D4E
C37	CAPR2W2,100pF		CAPR2W2
SW1	DIL(SW8),DIL(SW8)		DIL16
SW2	DIL(SW8),DIL(SW8)		DIL16
P1-5	POINT,POINT		Wiring pin
CO1	9-way Cannon Socket (FP)	9WCANBD	BITBUS Connr.
RN1	RN8COM,10K		SIL9
RN2	RN8COM,10K		SIL9
RN3	RN8COM,10K		SIL9
RN4	RN8COM,470R		SIL9
FS1	Littelfuse 3A		FUSECMC
JP1	JUMPER,JP		JP.1
JP2	JUMPER,JP		JP.1