

Dataway Test Module

DTM4

A.2956-7

CAMAC Bulletin classification group 4.

The DTM4 stores the state of the dataway bus lines and provides an LED display for manual troubleshooting, and read-back of the stored signals for computer-controlled systems check-out.

General description

The DTM4 Dataway Test Module is a single width CAMAC module which stores the states of the dataway Write, Read and Command lines in internal registers. The state of the registers is displayed on 67 front panel LED's. The contents of the Write and Command registers can be fed onto the dataway read lines. This module is an improved version of the DTM3, which it replaces. It is also very convenient for use as a test adjunct in the GEC-Elliott System Crate.

Using the DTM4

The dataway Read, Write, X and Q lines are continuously monitored and, at strobe S1, their respective registers are updated. The other dataway lines, except S1 and S2, have their registers updated at S1 and S2 of each dataway cycle. S1 and S2 strobe themselves.

The contents of all the register are continuously displayed on the front panel by light emitting diodes (LED's). A LAM trigger input sets a LAM status register which is controlled and tested using the register addressing method, and which includes the ability to set the LAM register by an addressed command.

The contents of the Write register can be fed onto the dataway Read lines with the command A(0).F(0). The register is cleared by

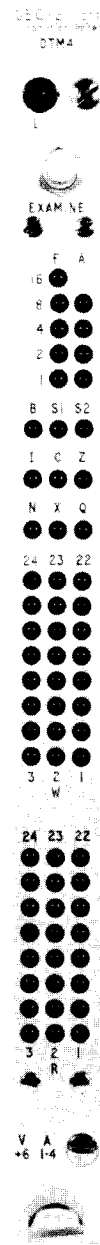
command A(0-15).F(9). The Command register contents can also be fed onto the dataway Read lines when addressed with A(1).F(0). While the Command register is being read the DTM4 is prevented from updating during that dataway cycle. The allocation of Read lines during a Command register read cycle is detailed in Table 1.

The Busy signal is delayed inside the module so that the S1 and S2 registers are not cleared when reading the Command register. This precaution is necessary because of the uncertainty of the time that N and B are generated before the S1 strobe in the dataway cycle. This delay is adjustable and is factory preset so that B occurs 250ns before S1 (measured at the rear panel socket). Adjustment of this delay might be required if controllers other than those of GEC-Elliott manufacture are used with the module.

Table 1 'Command' state read line allocation

| Read Line | Command | Read Line | Command |
|-----------|---------|-----------|---------|
| R1        | F1      | R9        | A8      |
| R2        | F2      | R10       | B       |
| R3        | F4      | R11       | N       |
| R4        | F8      | R12       | S1      |
| R5        | F16     | R13       | S2      |
| R6        | A1      | R14       | Z       |
| R7        | A2      | R15       | C       |
| R8        | A4      | R16       | I       |

The module can be used to monitor the state of the GEC-Elliott System Crate Dataway during a Branch cycle. This facility is enabled by the command S1.B. The re-allocation of Write lines for this application is detailed in Table 2.



during GEC-Elliott System Crate operation.

| WRITE LINE(W) | COMMAND SIGNAL |                            |
|---------------|----------------|----------------------------|
| 1             | N1             |                            |
| 2             | N2             |                            |
| 3             | N4             | Station Number             |
| 4             | N8             |                            |
| 5             | N16            |                            |
| 6             | C1             |                            |
| 7             | C2             | Single crate address       |
| 8             | C4             |                            |
| 9             | CAR            | Crate address register     |
| 10            | SR             | Stock register             |
| 11            | G              | Grant                      |
| 12            | B1             |                            |
| 13            | B2             | Branch code                |
| 14            | B4             |                            |
| 15            | Not used       |                            |
| 16            | T              | Timing (Branch mode)       |
| 17            | Not used       |                            |
| 18            | Not used       |                            |
| 19            | IDC1           |                            |
| 20            | IDC2           |                            |
| 21            | IDC3           | Indirect data channel code |
| 22            | IDC4           |                            |
| 23            | IDC5           |                            |
| 24            | IDC6           |                            |

A front panel push-button, 'Examine', allows the quiescent state of the dataway to be examined, with the exception of S1 and S2, whose internal registers are cleared. The button also resets the LAM status register.

### Signal monitoring

The dataway S1, S2, B, C, Z, I and OV lines are fed out to rear panel sockets for monitoring purposes. Sockets are also provided for LAM trigger and DMA SYNC LAM signals.

### Examine pushbutton

This control is located on the module front panel and enables the quiescent dataway state to be examined on the front panel LED's. The S1 and S2 registers are cleared when the push-button is operated and are not shown on the LED's. The EXAMINE control also resets the LAM status.

### Block diagram

A block diagram of the DTM4 is shown in Fig.1.

### Command structure

#### Addressed commands

These are detailed in Table 3.

#### Non-addressed commands

These are detailed in Table 4.

#### Data format

The data format of the Read lines when used for transmitting the stored command states is detailed in Table 1.

The re-allocated use of the Write lines during GEC-Elliott System Crate operation is detailed in Table 2.

### Facilities

#### Inputs

LAM Trigger

Signal Class: TTL pulled up via 7.5kΩ

Connector: Harwin W3000 socket mounted on rear panel.

#### Outputs

DMA LAM SYNC

Signal Class: TTL Totem pole (emitter follower sourcing and saturated transistor sinking current as opposed to free collector).

Dataway Monitoring Points

Dataway Signals: S1, S2, B, C, Z, I and OV

Signal Class: Un-buffered dataway signals

Connectors: Harwin W3000 socket mounted on rear panel

### Switches

EXAMINE: Pushbutton mounted on front panel. When operated the state of the dataway signals, except S1 and S2, is displayed on the front panel LED'S

### Links

Internal link pins allow the S1 and S2 signals to be either latched or displayed as stretched signals using internal monostables. The stretched signals' duration is determined by the value of the monostable capacitors fitted. The module is factory preset to the latched mode of operation.

### Indication

67 LED's mounted on the front panel indicating the following dataway signals:  
 24 Read  
 24 Write  
 5 Function  
 4 Sub-Address  
 1 each for N, B, S1, S2, C, Z, I, O, X, L.

### Mechanical

Single-width CAMAC module fully screened with hard-anodised aluminium panels.

### Power requirements

+6V 1.4A

Table 3 Addressed Commands

| COMMAND  | DESCRIPTION  | REMARKS (See note 1)               |
|--|--|------------------------------------|
| A(0).F(0)  | Read "Write" Register  | Clears LAM STATUS                  |
| A(1).F(0)  | Read "Command" Register  |                                    |
| A(0-15).F(9)   | Clear "Write" Register   |                                    |
| A(12).F(1)<br>A(12).F(19)<br>A(12).F(23)<br>A(13).F(1)<br>A(13).F(19)<br>A(13).F(23)<br>A(14).F(1)<br>A(15).F(8) | Read LAM Status Register via R1<br>Selective Set LAM Status Register<br>Selective Clear LAM Status Register<br>Read LAM Mask Register via R1<br>Selective Set LAM Mask Register<br>Selective Clear LAM Mask Register<br>Read LAM requests via R1<br>Test L | O = 1 if L = 1<br>L = N, L dataway |

Note 1 X response produced to all the Addressed Commands.

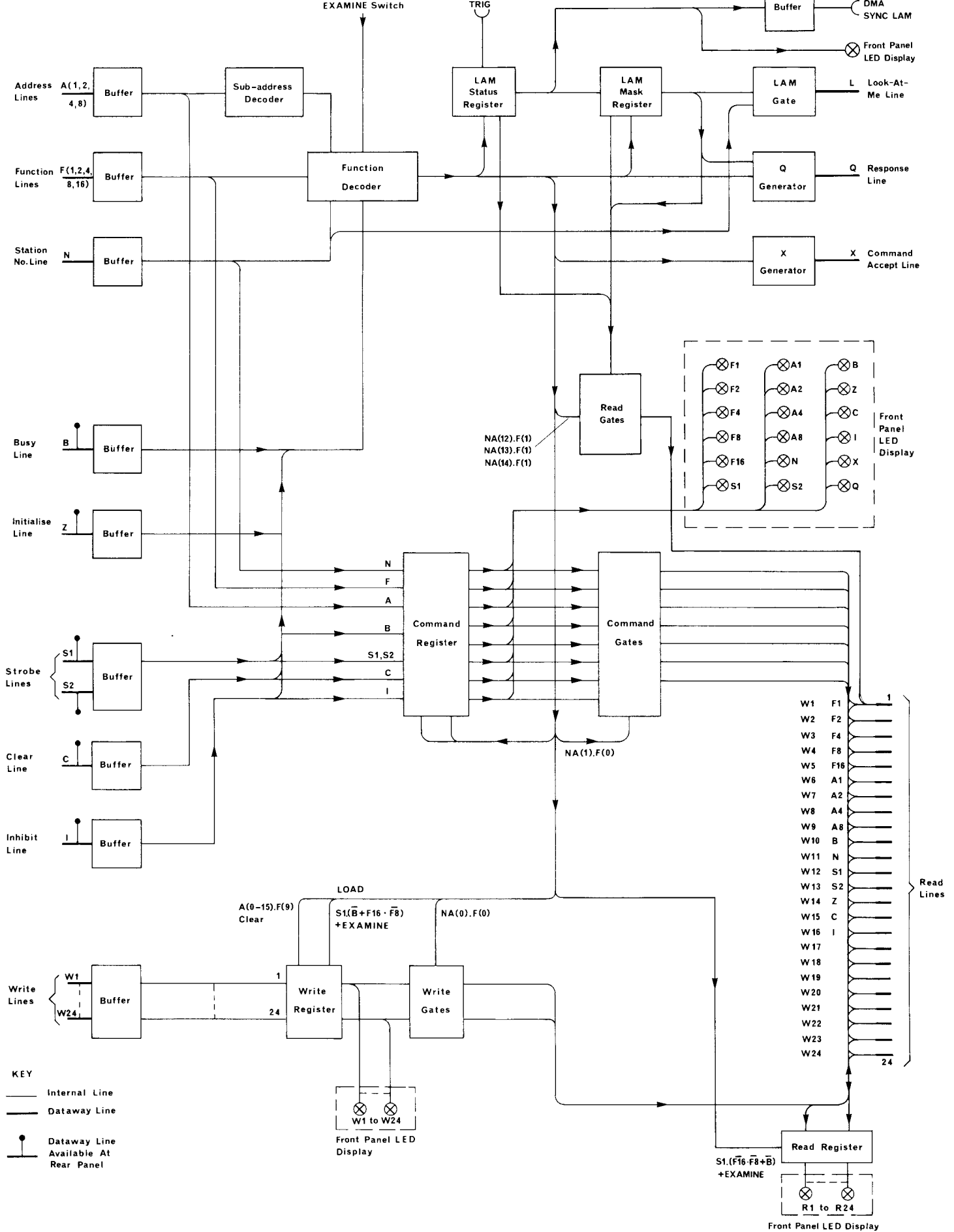


FIG 1 BLOCK DIAGRAM

(see Notes 1 and 2)

| COMMAND                     | DESCRIPTION             |
|-----------------------------|-------------------------|
| S1, (B + F16, F8) + Examine | Load "Read" Register    |
| S1, (B + F16, F8) + Examine | Load "Write" Register   |
| S1 + S2 + Examine           | Load "Command" Register |

- Note 1. Z,S2 Clears LAM Status Register and LAM Mask Register  
2. C and I not used.

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